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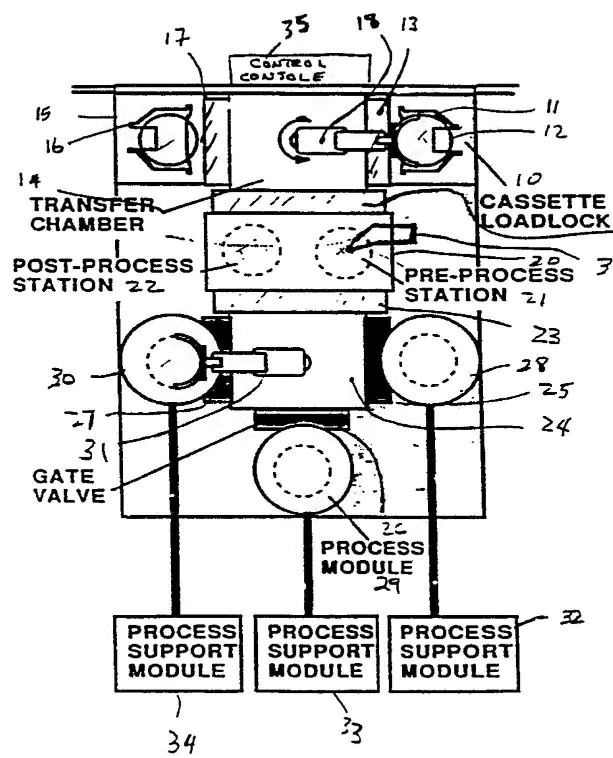
(54) Title: AUTOMATED WAFER TRANSPORT SYSTEM

(57) Abstract

Program control transportation of semiconductor wafers (12) or other substrates among a plurality of reaction chambers (28), (29), (30). The apparatus comprises a cassette loadlock (10) for docking a cassette (11) holding a plurality of wafers (12). A first transfert chamber (14) having a plurality of gates (13), (17), (19), one of which is coupled to the cassette loadlock (10), transfers wafers (12) through the plurality of gates (13), (17), (19). A second transfer chamber (24), has a plurality of gates (23), (25), (26), (27) connected to process stations (28), (29), (30). A staging chamber (20) includes incoming and outgoing staging stations (21), (22) and is connected by gates (19), (23) to the first and second transfer stations (14), (24). There are first and second robotic arms (18), (31) in the first and second transfer chambers (14), (24) to transfer wafers (12) between the loadlock (10), the staging chamber (20), and the process stations (28), (29), (30). A monitor system (36) is mounted with the staging chamber (20). The system is modular and can be expanded both vertically and horizontally.



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AUTOMATED WAFER TRANSPORT SYSTEM

Background of the Invention

Field of the Invention

The present invention relates to automated wafer transport systems used for processing semiconductor wafers during the manufacture of integrated circuits.

Description of Related Art

Automated single wafer transport systems are utilized in the manufacture of integrated circuits, to transport wafers of semiconductor material between process chambers, such as chemical vapor deposition chambers, annealing chambers, and etching chambers. The wafers are typically transported in a cassette that contains a number of wafers in a clean room environment from one process chamber to the next. Some systems consist of a cassette loadlock and a robotic transfer chamber with a robotic arm which removes individual wafers from the loadlock and transports them to one or more process chambers coupled with the

robotic transfer chamber.

These prior art automated wafer transport systems have suffered the disadvantage that they have been individually designed to meet the needs of particular process systems. Thus, expansion of the transport systems has proved impractical.

In addition, the prior art wafer transport systems which serve a plurality of process stations have experienced gridlock situations, where movement of wafers into and out of the process stations is slowed to a crawl because of the limited availability of paths into and out of the respective stations.

Accordingly, there is a need for an automated single wafer transport system that is expandable and that provides for greater throughput of wafers, particularly in the expanded systems.

Summary of the Invention

The present invention provides an apparatus for automated transport of wafers, or other process substrates, among a plurality of reaction chambers. The apparatus comprises two cassette docks for docking a cassette holding a plurality of wafers. A first robotic transfer chamber having a first plurality of gates, two of which are coupled to respective cassette

docks, transports wafers through the plurality of gates. A second robotic transfer chamber, having a second plurality of gates, transports wafers through the second plurality of gates. A plurality of process stations is mounted with the apparatus, each coupled to one or more of the second plurality of gates of the second robotic chamber. A staging chamber is coupled to one of the first plurality of gates on the first robotic transfer chamber, and to one of the second plurality of gates on the second robotic chamber. The staging chamber includes a plurality of stations for staging the wafers and is used for transportation of wafers from the first robotic transfer chamber into the second robotic transfer chamber. Accordingly, at least one of the stations in the staging chamber can be used for incoming pre-process wafers while another of the stations can be used for outgoing post-process wafers.

According to a second aspect of the invention, a monitor system and/or preparing/finishing apparatus is mounted with the staging chamber, for monitoring and/or preparing/finishing a characteristic of wafers in either a pre-process or post-process station.

In addition, a programmable control console, which is coupled to the wafer transport system and the process stations, controls the transportation of single wafers through the stations in the staging chamber, the

process stations, and the cassette. The programmable control console may also be coupled to the monitor mounted with the staging chamber, for providing further input to the transportation control process.

According to a further aspect of the present invention, the staging chamber provides for a modular interface between the robotic chambers that allows for unlimited expansion of the system. In particular, the system referred to above could have a second staging chamber coupled to one of the gates in the second robotic chamber. According to this aspect, a third robotic transfer chamber is coupled to the second staging chamber and to a plurality of other process stations. The second staging chamber also includes at least two staging stations, so that wafers moving into the third robotic chamber are not blocked by wafers being moved out and vice-versa. This aspect allows for vertical expansion of the system.

According to another aspect of the invention, a second staging chamber is coupled to one of the first plurality of gates of the first robotic transfer chamber and to a third robotic transfer chamber. The third robotic chamber may be coupled to a second transportation system through a similar second staging chamber. This aspect allows for horizontal expansion of the wafer transport system.

Other aspects and advantages of the invention can be seen by review of the figures, the detailed description, and the claims which follow.

Brief Description of the Figures

Fig. 1 is a schematic diagram of a single wafer transportation system according to the present invention.

Fig. 2 is a schematic diagram of a single wafer transportation system according to the present invention which has been vertically expanded using the modular staging chamber and robotic transfer chamber.

Fig. 3 is a schematic diagram of a single wafer transportation system according to the present invention which has been horizontally expanded.

Fig. 4 is a flow chart illustrating the control algorithm followed in moving a wafer from an entry stage through a process station and back to the exit elevator.

Fig. 5 is a flow chart illustrating operation of the "place wafer on entry stage" step shown in Fig. 4.

Fig. 6 is a flow chart illustrating operation of the "place wafer on IA (inner arm)" step of Fig. 4.

Fig. 7 is a flow chart illustrating operation of the "place wafer in P1 (process station one)" step of

Fig. 4.

Fig. 8 is a flow chart illustrating operation of the "remove wafer from P1" step of Fig. 4.

Fig. 9 is a flow chart illustrating operation of the "place wafer on exit stage, then on OA (outer arm)" step of Fig. 4.

Fig. 10 is a flow chart illustrating operation of the "place wafer in EX ELEV (exit elevator)" of Fig. 4.

Detailed Description

A detailed description of preferred embodiments of the present invention is described with reference to the figures.

A single wafer transport system according to the present invention is set out in Fig. 1. The system includes a first cassette dock 10 for staging a cassette 11 of semiconductor wafers 12 into the system. Alternatively, the dock 10 may be adapted for single wafers, SMIF compartments, or for other process substrates. The cassette dock 10 is coupled at gate 13 with a first robotic transfer chamber 14. The gate may or may not include a valve for isolating the cassette dock 10 from the transfer chamber 14. In the preferred system, the cassette dock includes an elevator inside a loadlock.

The system includes a second cassette dock 15 for staging wafers in a cassette 16 through a gate 17 which is coupled to the first robotic transfer chamber 14. The first robotic transfer chamber 14 includes a robotic arm 18 for transporting wafers through the valve gates 13 and 17, and through a third gate 19 into a staging chamber 20.

The staging chamber 20 includes a plurality of stations for staging wafers into the process modules. In particular, a pre-process station 21 and a post-process station 22 are provided for supporting wafers in the staging chamber 20. The staging chamber 20 is coupled to a gate 23 of a second robotic transfer chamber 24. The second robotic transfer chamber includes a plurality of valve gates 25, 26, 27 which are coupled to process chambers 28, 29, 30. A robotic arm 31 in the second robotic transfer chamber 24 transfers wafers from the pre-process station into individual process chambers 28, 29, 30, and out of the process chambers 28, 29, 30, into the post-process station 22 of the staging chamber 20. The robotic arm 18 in the first robotic transfer chamber 14 then completes the transportation of the wafer from the staging chamber 20 into a cassette in a cassette dock 10 or 15.

Coupled to each of the process chambers 28, 29,

30, is a process support module 32, 33, 34 which is particularly adapted to support a given process in a respective process chamber.

A control console 35 made up of a programmable computer, is coupled to the robotic arms 18, 31, the gates 13, 17, 19, 23, 25, 26, 27, the pre- and post-process stations 21, 22, the cassette docks 10, 15, a variety of sensors not shown here, and to the process support modules 32, 33, 34, and controls the transportation of single wafers through the system under program control. A preferred control algorithm is described below with reference to Figs. 4-10.

The staging chamber 20 having a plurality of staging stations facilitates the transportation of wafers into the process chambers while avoiding gridlock between ingoing and outgoing wafers.

In addition, a mechanism 36 comprising monitoring, preparation and/or finishing apparatus is coupled with the staging chamber 20. The mechanism 36 is schematically illustrated in Fig. 1, but may comprise any of a variety of systems for monitoring a characteristic of a wafer, preparing the wafer or finishing a process of the wafer sitting in one of the plurality of stations 21, 22 of the staging chamber 20. For instance, the apparatus 36 could be a system for detecting cleanliness of the wafer, a system for

reading an identifying marker on the wafer for inventory processes, an eyepiece for visual inspection of the wafer, or other characteristic monitoring apparatus known in the art. Examples of "preparation" steps that could be done by mechanism 36 include preparing the wafer to a designated location or orientation, and conditioning or cleaning of the surface of the wafer. Examples of "post" or "finishing" processes include measuring the result of process, and heating or cooling of the substrate. For a mechanism 36 that generates a monitor or process status signal, the mechanism 36 is coupled to the control console 35 providing input to the transportation control system.

Fig. 2 illustrates a vertical expansion of the wafer transport system shown in Fig. 1. The reference numbers used in Fig. 1 are repeated for similar elements.

Accordingly, the system shown in Fig. 2 includes a first cassette dock 10 and a second cassette dock 15. The cassette 11 of semiconductor wafers 12 is loaded in the cassette dock 10. Also, a cassette 16 of wafers is loaded in dock 15. A first robotic transfer chamber 14 supports a robotic arm 18 which is used to transfer wafers through the gates 13, 18, and 19 of the first robotic transfer chamber 14. The gate 19 is coupled to

the staging chamber 20 which includes a plurality 21, 22 of staging stations. The staging chamber 20 is coupled to gate 23 of a second robotic transfer chamber 24. The second robotic transfer chamber 24 includes gates 25, 27 which are coupled to process chambers 28, 30. In addition, a gate 100 on the second robotic transfer chamber 24 is coupled to a second staging chamber 101. The staging chamber 101 includes a plurality of staging stations 102, 103.

The staging chamber 101 is coupled to a gate 104 on third robotic transfer chamber 105. A robotic arm 106 in the third robotic transfer chamber 105 transfers wafers from the second staging chamber 101 through a plurality of gates 104, 107, 108, 109 to respective process chambers 110, 111, 112. The control console 35 is coupled to the first, second and third robotic transfer chambers 105, 24, 14, other elements of the system, and to the process modules (not shown) which are coupled to each of the process chambers. Under program control, wafers are transported through the transportation system to the appropriate process chambers.

As can be seen, the system provides for two way traffic of single wafers through the chambers. Thus, a wafer can enter from cassette dock 10 and be placed on a pre-process station 21. From station 21, the wafer

can be placed in process chamber 28. After processing in chamber 28, the wafer can be transported to staging station 102. From staging station 102, the wafer can be moved into process chamber 110, then process chamber 111, then process chamber 112. From chamber 112, the wafer can be transported to the staging station 103. From staging station 103, the robotic arm 31 in the second robotic transfer chamber 24 can transport the wafer into process chamber 30. From chamber 30, the wafer can be transported to staging station 22. From staging station 22, the wafer can be transported to the outgoing cassette 16 in the cassette dock 15.

The modularity of the system according to the present invention is further illustrated by the horizontal expansion capability shown in Fig. 3. According to the horizontal expansion capability, the wafer transport system includes a cassette dock 200 for supporting a cassette 201 of semiconductor wafers. The cassette dock 200 is coupled to gate 202 of a first robotic transfer chamber 203. First robotic transfer chamber 203 includes a second gate 204 and a third gate 205. The third gate 205 is coupled to a staging chamber 206 having a plurality of wafer staging stations 207, 208. The staging chamber 206 is coupled to gate 209 of a second robotic transfer chamber 210. The second robotic transfer chamber 210 includes a

plurality of gates 211, 212, 213 to which respective process chambers 214, 215, 216 are coupled.

A robotic arm 217 in the first robotic transfer chamber 203 transfers wafers through the plurality of gates 202, 204, 205 of the first robotic transfer chamber 203. A robotic arm 218 of the second robotic transfer chamber 210 is used to transfer wafers from the staging stations 207, 208 into the process chambers 214, 215, 216 through the second plurality of gates 211, 212, 213.

Coupled to the first robotic transfer chamber 203 at gate 204 is a staging chamber 220 including a staging station 221. The staging chamber 220 is coupled to gate 222 of a third robotic transfer chamber 223. Third robotic transfer chamber 223 includes a second gate 224 coupled to a staging chamber 225 on a second wafer transfer system. The staging chamber 225 includes a staging station 226 for receiving wafers from the third robotic transfer chamber 223. A fourth robotic transfer chamber 227 is coupled through gate 228 to the staging chamber 225, and through gate 230 to the cassette dock 229.

The staging chamber 231 and fifth robotic transfer chamber 232 are mounted as is described with reference to the parallel system.

In the horizontally expanded system shown in Fig.

3, the control console 240 is coupled to the first system and controls the first, second, and third transfer chambers 203, 210, 223. A second control console 241 is coupled to the third, fourth, and fifth transfer chambers 223, 227, 232. A simple contention algorithm may control operation of the third transfer chamber 223 in order to coordinate the activity of the two parallel systems. Alternatively, a single control console could operate both systems.

Figs. 4-10 set out a description of a preferred embodiment of a control algorithm based on petri net theory. Fig. 4 shows the master structure of the control net for moving a wafer from an entry elevator through a process station and back out to the exit elevator. Figs. 5-10 show additional detail of the activities set out in Fig. 4.

With reference to Fig. 4, an overall view of the control net is shown. The net is begun at Start_Petri point 400 which is passed to the Place Wafer on Entry Stage activity 401 to place the wafer on the entry stage. The output of the activity 401 is a Wafer on the EN STAGE signal 402.

The Wafer on EN STAGE signal 402 is passed to the Place Wafer on IA activity 403 of placing the wafer on the inner arm (corresponding to the robotic arm 31 of Fig. 1).

The Place Wafer on IA activity 403 is linked to an EN_STG_Free semaphore 405, indicating that the entry stage is free, and the OA_Free semaphore 406 indicating that the outer arm is free. These semaphores 405, 406 are linked back to the activity 401, and OA_Free semaphore 406 is linked back to activity 413.

The Wafer on IA, IA Retracted output 404 of the activity 403 indicates that a wafer is on the inner arm and the inner arm has been retracted. This signal 404 is passed to Place Wafer in P1 & Process activity 407 by which the wafer is moved into a process station and processed.

The Place Wafer in P1 & Process activity 407 is linked to the IA_Free semaphore 408 indicating that the inner arm is free. This semaphore is linked back to activities 403 and 410. The result of Place Wafer in P1 & Process activity 407 is a P1 Finished Process signal 409 indicating that process station 1 has finished processing the wafer. Signal 409 is passed to Remove Wafer from P1 activity 410. This activity 410 is linked to a P1_Free semaphore 411 which is linked back to the activity 403.

The output of the Remove Wafer from P1 activity 410 is a Wafer on IA signal 412 indicating that the wafer is on the inner arm. This signal 412 is passed

to Place Wafer on Exit Stage then on OA activity 413.

The Place Wafer on Exit Stage then on OA activity 413 generates the Wafer on OA signal 414, and is linked to the IA_Free semaphore 408.

The Wafer on OA signal 414 is passed to the Place Wafer on EX ELEV activity 415. As a result of the Place Wafer on EX ELEV activity 415, the control net is completed for the given wafer at End_Petri point 416.

The Place Wafer on EX ELEV activity 415 is linked to the Yes_More_Slots semaphore 417 which is linked back to activity 413, and the EX_STG_Free semaphore 418 which is linked back to activity 410. Also, it is linked to the OA_Free semaphore 406.

The IA_Free semaphore 408 is linked back to both activities 403 and 410. The OA_Free semaphore 406 is linked back to both activities 401 and 413.

Each of the activities 401, 403, 407, 410, 413 and 415 of Fig. 4 is broken down in more detail in Figs. 5-10, respectively.

Fig. 5 illustrates the Place Wafer on Entry Stage activity 401. Inputs include the Start_Petri signal 400, the EN_STAGE_Free semaphore 405, and the OA_Free semaphore 406. The output is the Wafer on EN STAGE signal 402.

The inputs Start_Petri 400, EN_STAGE_Free 405, and OA Free 406 are supplied to the Ext_OA_EN_ELV0 activity

500. This activity generates an output at point 501 which is coupled to the Stp_Dn_EN_ELEV activity 502. The activity 502 is linked to the Yes_More_Wfrs semaphore 503 and the EN_ELEV_at_Slt semaphore 504.

The output of the activity 502 is the Wafer on OA signal 505. The Wafer on OA signal 505 is passed to the Rtr_OA_EN_ELV1 activity 506. After the outer arm is retracted from the entry elevator in activity 506, a signal 507 is passed to the Ext_OA_EN_STG1 activity 508. After the outer arm is extended to the Entry Stage, signal 509 is passed to the Rse_EN_STGE activity 510. After the Entry Stage has risen to lift the wafer off of the outer arm, the Wafer on EN STAGE signal 402 is generated.

Fig. 6 illustrates the Place Wafer on IA activity 403. Inputs include the Wafer on EN STAGE signal 402, the P1_Free semaphore 411, and the IA_Free semaphore 408. Outputs include a link to the OA_Free semaphore 406, a link to the EN_STAGE Free semaphore 405, and the Wafer on IA, IA Retracted signal 404.

The Wafer on EN STAGE signal 402 is supplied to the Rtr_OA_EN_STG0 activity 600. After the outer arm is retracted from the entry stage, signal 601 is passed to the Ext_IA_EN_STG0 activity 602 and the OA_Free semaphore 406 is updated. If process 1 is free and the inner arm is free as indicated by the respective

semaphores 411 and 408, the inner arm is extended to the Entry Stage and the signal 603 is passed to the Lwr_EN_STGE activity 604. The entry stage is lowered to pass the wafer to the inner arm and the Wafer on IA signal 605 is passed to the Rtr_IA_EN_STG1 activity 606. After the inner arm is retracted from the Entry Stage, the Wafer on IA, IA Retracted signal 404 is generated and the EN_STGE_Free semaphore 405 is updated.

Fig. 7 illustrates the Place Wafer on P1 activity 407. Inputs include the Wafer on IA, IA Retracted signal 404. Outputs include the P1 Finished Process signal 409 and a link to the IA_Free semaphore 408.

The Wafer on IA, IA Retracted signal 404 is passed to the Opn_P1_GTE_VLV activity 700. After the Process Station 1 gate valve is open, the signal 701 is passed to the Ext_IA_P11 activity 702. After the inner arm is extended to Process Station 1, a signal 703 is passed to the Rse_P1 activity 704. After the Process Station P1 picks up the wafer, a signal 705 is passed to the Rtr_IA_P10 activity 706. After the inner arm is retracted from Process Station 1, the IA_Free semaphore 408 is updated and a signal 707 is passed to the Cls_P1_GTE_VLV activity 708. After the Process Station 1 gate valve is closed, a signal 709 is passed to the Process_P1 activity 710. When the process is

complete, the P1 Finished Process signal 409 is generated.

Fig. 8 illustrates the Remove Wafer from P1 activity 410. The inputs include the P1 Finished Process signal 409, the EX_STG_Free semaphore 418, and the IA_Free semaphore 408. Outputs include the Wafer on IA signal 412 and a link to the P1_Free semaphore 411.

The P1 Finished Process signal 409 is passed to the Opn_P1_GTE_VLV activity 800. After the gate valve on Process Station 1 is open, the signal 801 is passed to the Ext_IA_P10 activity 802. If the Exit Stage is free, and the inner arm is free, then the inner arm is extended into the Process Station to pick up the wafer. When extended, the signal 803 is passed to the Lwr_P1 activity 804. After P1 stage is lowered, placing the wafer on the inner arm, the signal 805 is passed to the Rtr_IA_P11 activity 806. After the inner arm is retracted from the Process Station, signal 807 is passed to the Cls_P1_GTE_VLV activity 808. When the gate valve of Process Station 1 is closed, the Wafer on IA signal 412 is generated. Also, the P1_Free semaphore 411 is updated.

Fig. 9 illustrates the Place Wafer on Exit Stage, then on OA activity 413. Inputs include the Wafer on IA signal 412, the Yes_More_Slots semaphore 417 and the

OA_Free semaphore 406. Outputs include the Wafer on OA signal 414 and a link to the IA_Free semaphore 408.

The Wafer on IA signal is passed to the Ext_IA_EX_STG1 activity 900. Once the inner arm is extended to the Exit Stage in the staging chamber, a signal 901 is passed to the Rse_EX_STGE activity 902. After the Exit Stage has risen to lift the wafer from the inner arm, a signal 903 is passed to the Rtr_IA_EX_STG0 activity 904. When the inner arm is retracted, the Wafer on EX STAGE signal 905 is passed to the Ext_OA_EX_STG0 activity 906, and the IA_Free semaphore 408 is updated.

If the Yes_More_Slots semaphore 417 is true, and the OA_Free semaphore 406 is true, the outer arm is extended to the Exit Stage and a signal 907 is passed by activity 906 to the Lwr_EX_STGE activity 908. When the Exit Stage has been lowered to place the wafer on the outer arm, the Wafer on OA signal 414 is generated.

Fig. 10 illustrates the Place Wafer in EX ELEV activity 415. The input includes the Wafer on OA signal 414. Outputs include the End Petri signal 416, a link to the EX_STGE_Free semaphore 418, a link to the Yes_More_Slots semaphore 417 and a link to the OA_Free semaphore 406.

The Wafer on OA signal 414 is passed to the Rtr_OA_EX_STG1 activity 1000. Once the outer arm is

retracted from the Exit Stage, the Ex_STGE_Free semaphore 418 is updated and a signal 1001 is passed to the Ext_OA_EX_ELV1 activity 1002. A second input to the activity 1002 is the EX_ELEV_at_Slt semaphore 1003. If the Exit Elevator is at the proper slot, when the signal 1001 is passed to activity 1002, then the outer arm is extended to the Exit Elevator and a signal 1004 is passed to the Rse_EX_ELEV activity 1005. The Exit Elevator is raised to lift the wafer off of the outer arm, and the Yes_More_Slots semaphore 417 and the Ex_ELEV_at_Slt semaphore 1003 are updated. Also, the End_Petri signal 416 is generated. In addition, a signal 1006 is passed to the Rtr_OA_EX_ELV0 activity 1007. Once the outer arm is retracted from the Exit Elevator, leaving the wafer in the elevator, the OA_Free semaphore 406 is updated.

As can be seen, the control algorithm is based on the classical Petri net control flow using activities, semaphores, and links between activities and semaphores.

The combination of the Petri net control flow and the wafer handling apparatus illustrated with respect to Figs. 1-3, provide a wafer handling system which can maximize the use of the available resources by avoiding gridlock, providing precise control for each activity, and allowing a modular approach to modifying control

algorithm to meet the needs of specific process sequences and specific wafer routes to one or more process chambers.

In sum, an automated single wafer transport system can be used to interface with several process specific chambers, such that a common transport system can be shared. The modularity allows interchange of process specific chambers on a single transportation system. The flexibility and expansion modularity can be used to accommodate a wide variety of processes. The pre- and post-process stations maximize handling through-put, eliminate gridlock, offer options for material and process verification monitoring, and offer convenient locations for the preparation and/or finishing of wafers in the process sequence.

The foregoing description of preferred embodiments of the present invention has been provided for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, thereby enabling others skilled in the art to understand the invention for various embodiments and

with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the following claims and their equivalents.

CLAIMS

1. An apparatus for automated transportation of substrates among a plurality of process chambers, comprising:

docking means for docking substrates;

first robotic means, having a first plurality of gates, one of which is coupled to the docking means, for transporting substrates through the first plurality of gates;

second robotic means, having a second plurality of gates, for transporting substrates through the second plurality of gates, wherein each of the plurality of process chambers is coupled to a respective one of the second plurality of gates; and

staging means, having a first gate coupled to one of the first plurality of gates, and having a second gate coupled to one of the second plurality of gates, for staging substrates for transportation by the first robotic means and the second robotic means the staging means including a plurality of stations for staging substrates.

2. The apparatus of claim 1, further including: control means, coupled to the first robotic means,

and the second robotic means, for controlling the transportation of single substrates through the stations in the staging means and the process chambers.

3. The apparatus of claim 1, further including: means, coupled with one station of the plurality of stations in the staging means, for monitoring a characteristic of substrates staged in the one station.

4. The apparatus of claim 3, further including: programmable control means, coupled to the first robotic means, the second robotic means, and the means for monitoring, for controlling the transportation of single substrates through the stations in the staging means and the process chambers.

5. The apparatus of claim 1, further including: means, coupled with one station of the plurality of stations in the staging means, for preparing substrates staged in the one station before a specified process in one of the plurality of process chambers.

6. The apparatus of claim 1, further including: means, coupled with one station of the plurality of stations in the staging means, for finishing substrates staged in the one station after a specified

process in one of the plurality of process chambers.

7. The apparatus of claim 1, further including:

second docking means, coupled to one of the first plurality of gates, for docking substrates.

8. The apparatus of claim 1, further including:

third robotic means, having a third plurality of gates, for transporting substrates through the third plurality of gates; and

second staging means, coupled to one of the first plurality of gates, and to one of the third plurality of gates, and having at least one staging station, for staging substrates for transportation by the first robotic means and the third robotic means.

9. The apparatus of claim 1, further including:

third robotic means, having a third plurality of gates, for transporting substrates through the third plurality of gates; and

second staging means, coupled to one of the second plurality of gates, and to one of the third plurality of gates, and having at least one staging station, for staging substrates for transportation by the second robotic means and the third robotic means.

10. An apparatus for automated transportation of substrates among a plurality of process chambers and at least one substrate storage cassette, comprising:

cassette docking means for docking a substrate storage cassette;

first robotic means, having a first plurality of gates, one of which is coupled to the cassette docking means, for transporting substrates through the first plurality of gates;

second robotic means, having a second plurality of gates, for transporting substrates through the second plurality of gates, wherein each of the plurality of process chambers is coupled to a respective one of the second plurality of gates;

staging means, coupled to one of the first plurality of gates, and coupled to one of the second plurality of gates, for staging substrates for transportation by the first robotic means and the second robotic means, the staging means including a pre-process station for staging substrates prior to processing in a process chamber, and a post-process chamber for staging substrates after processing; and

programmable control means, coupled to the first robotic means, and the second robotic means, for controlling the transportation of single substrates through the pre-′ and post- stations in the staging

means, the process chambers, and the cassette docking means.

11. The apparatus of claim 10, further including:

means, coupled with the pre-process station in the staging means, for monitoring a characteristic of substrates staged in the pre-process station.

12. The apparatus of claim 10, further including:

means, coupled with the post-process station in the staging means, for monitoring a characteristic of substrates staged in the post-process station.

13. The apparatus of claim 11, wherein the means for monitoring includes means for generating a monitor signal and the programmable control means is connected to the means for monitoring and responsive the monitor control signal, for controlling transportation of substrates to and from the pre-process station.

14. The apparatus of claim 12, wherein the means for monitoring includes means for generating a monitor signal and the programmable control means is connected to the means for monitoring and responsive the monitor control signal, for controlling transportation of substrates to and from the post-process station.

15. The apparatus of claim 10, further including: means, coupled with the pre-process station in the staging means, for preparing substrates staged in the pre-process station before a specified process in one of the plurality of process chambers.

16. The apparatus of claim 10, further including: means, coupled with the post-process station in the staging means, for finishing substrates staged in the post-process station before the substrate is passed to the cassette docking means.

17. The apparatus of claim 10, further including: second cassette docking means, coupled to one of the first plurality of gates, for docking a second substrate storage cassette.

18. The apparatus of claim 10, further including: third robotic means, having a third plurality of gates, for transporting substrates through the third plurality of gates; and

second staging means, coupled to one of the first plurality of gates, and to one of the third plurality of gates, and having at least one staging station, for staging substrates for transportation by the first

robotic means and the third robotic means.

19. The apparatus of claim 10, further including:

third robotic means, having a third plurality of gates, for transporting substrates through the third plurality of gates; and

second staging means, coupled to one of the second plurality of gates, and to one of the third plurality of gates, and having at least one staging station, for staging substrates for transportation by the second robotic means and the third robotic means.

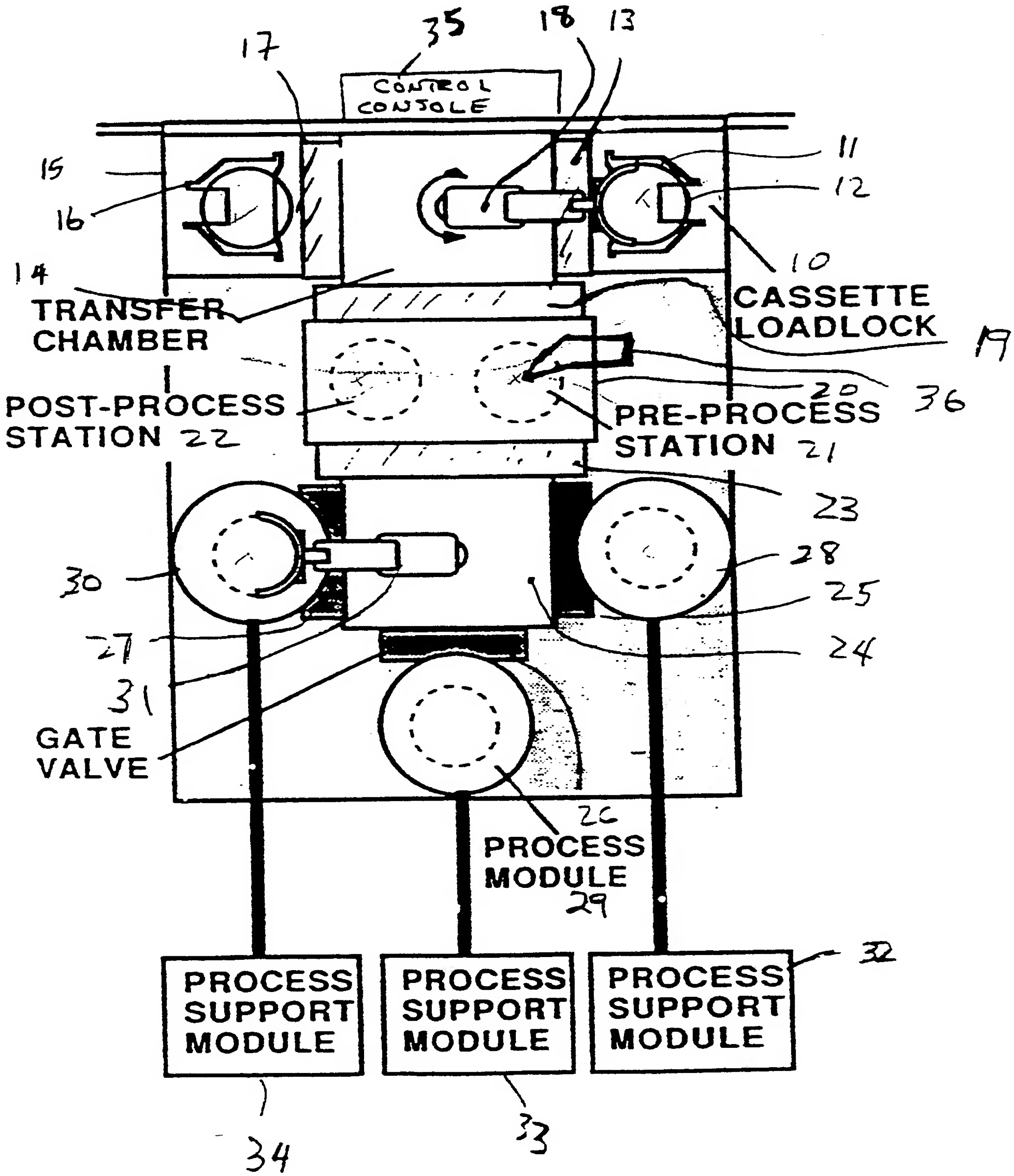

35
18
13
17
CONTROL CONSOLE
11
15
12
16
10
14
TRANSFER CHAMBER
CASSETTE LOADLOCK
19
36
20
POST-PROCESS STATION 22
PRE-PROCESS STATION 21
23
28
30
25
27
24
31
GATE VALVE
26
PROCESS MODULE
29
32
PROCESS SUPPORT MODULE
PROCESS SUPPORT MODULE
PROCESS SUPPORT MODULE
34
33

FIG 1

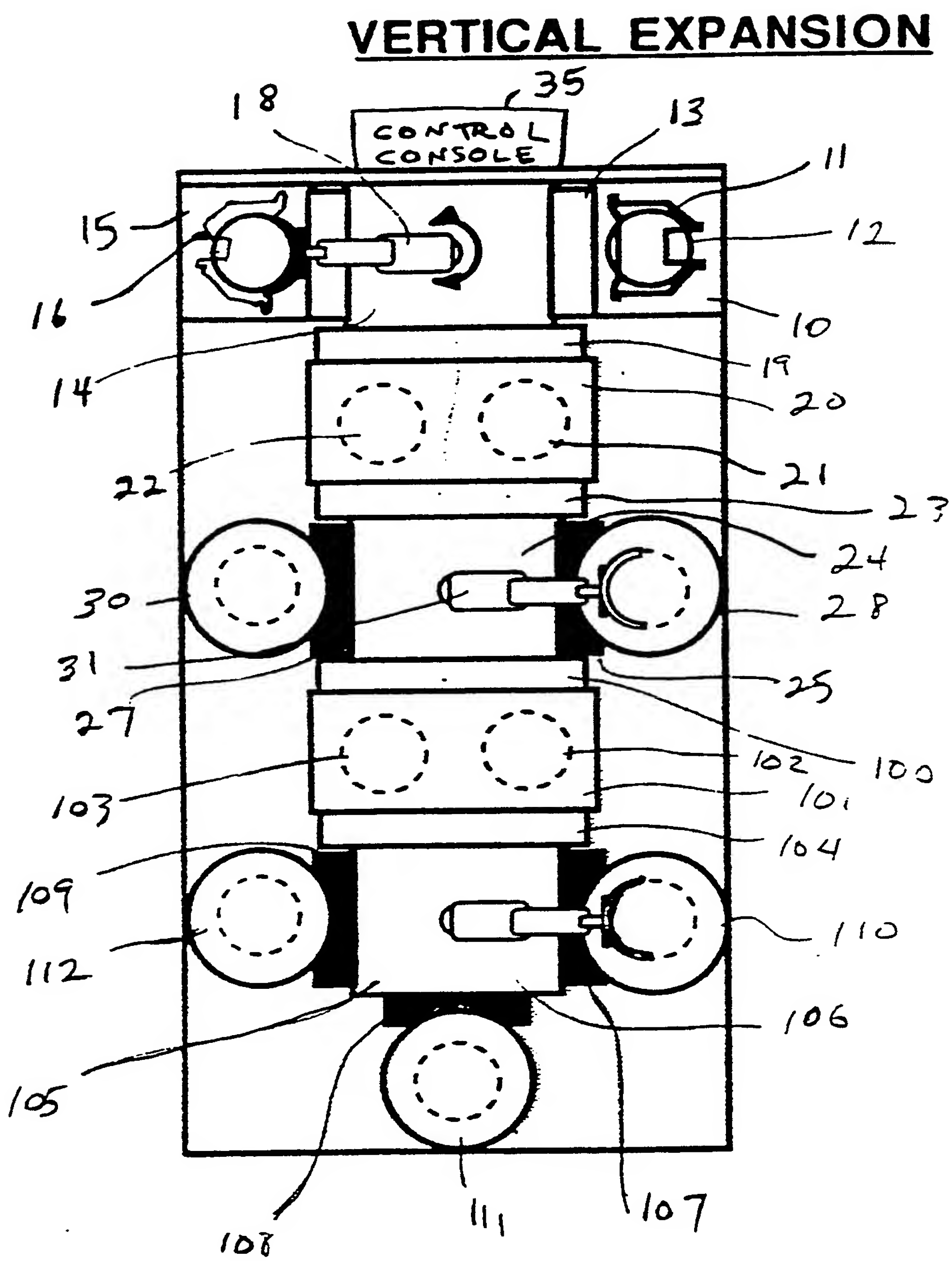

VERTICAL EXPANSION
35
CONTROL CONSOLE
18
13
11
15
12
16
10
14
19
20
22
21
23
24
30
28
31
25
27
102
100
103
101
104
109
110
112
106
105
108
111
107

FIG 2

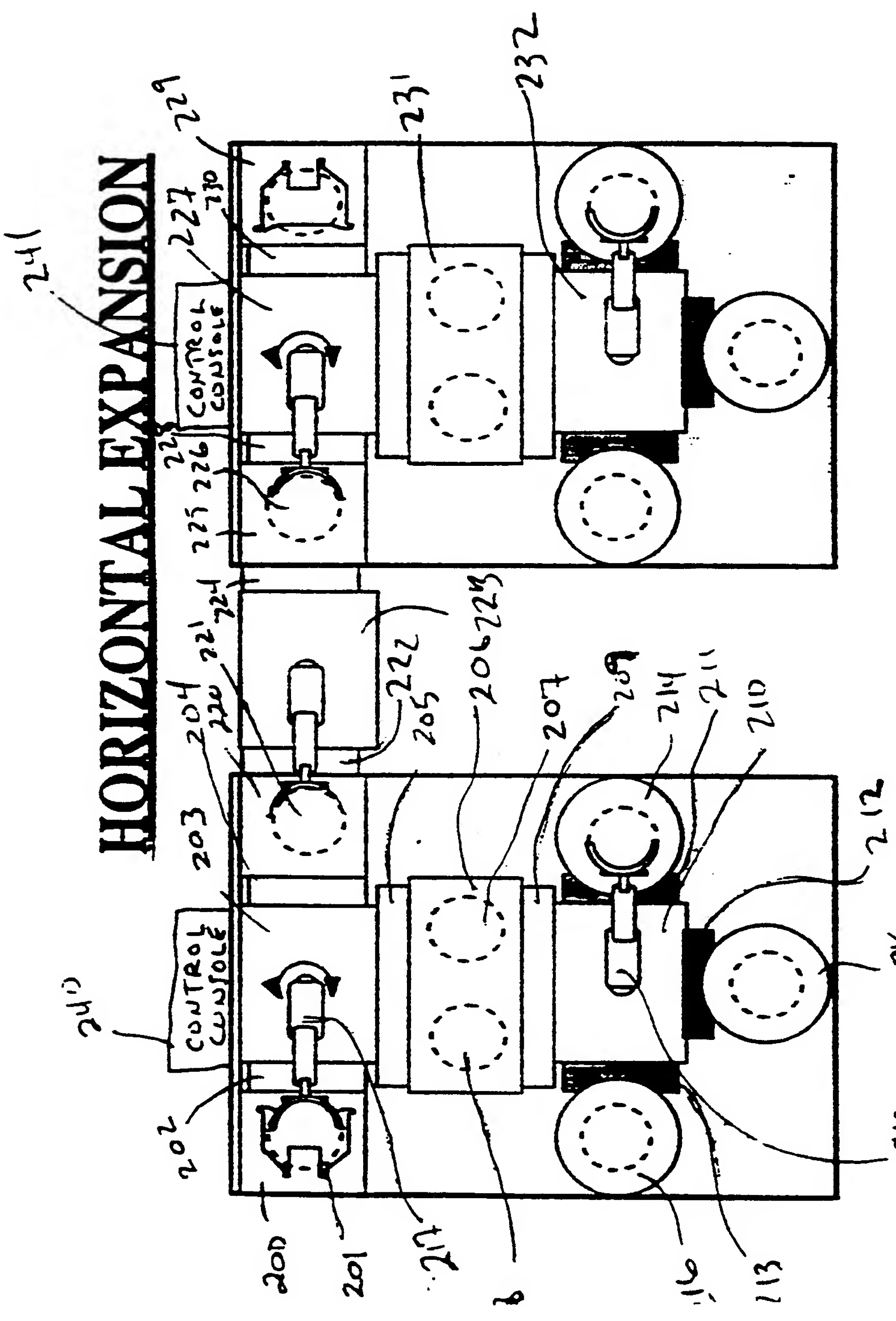
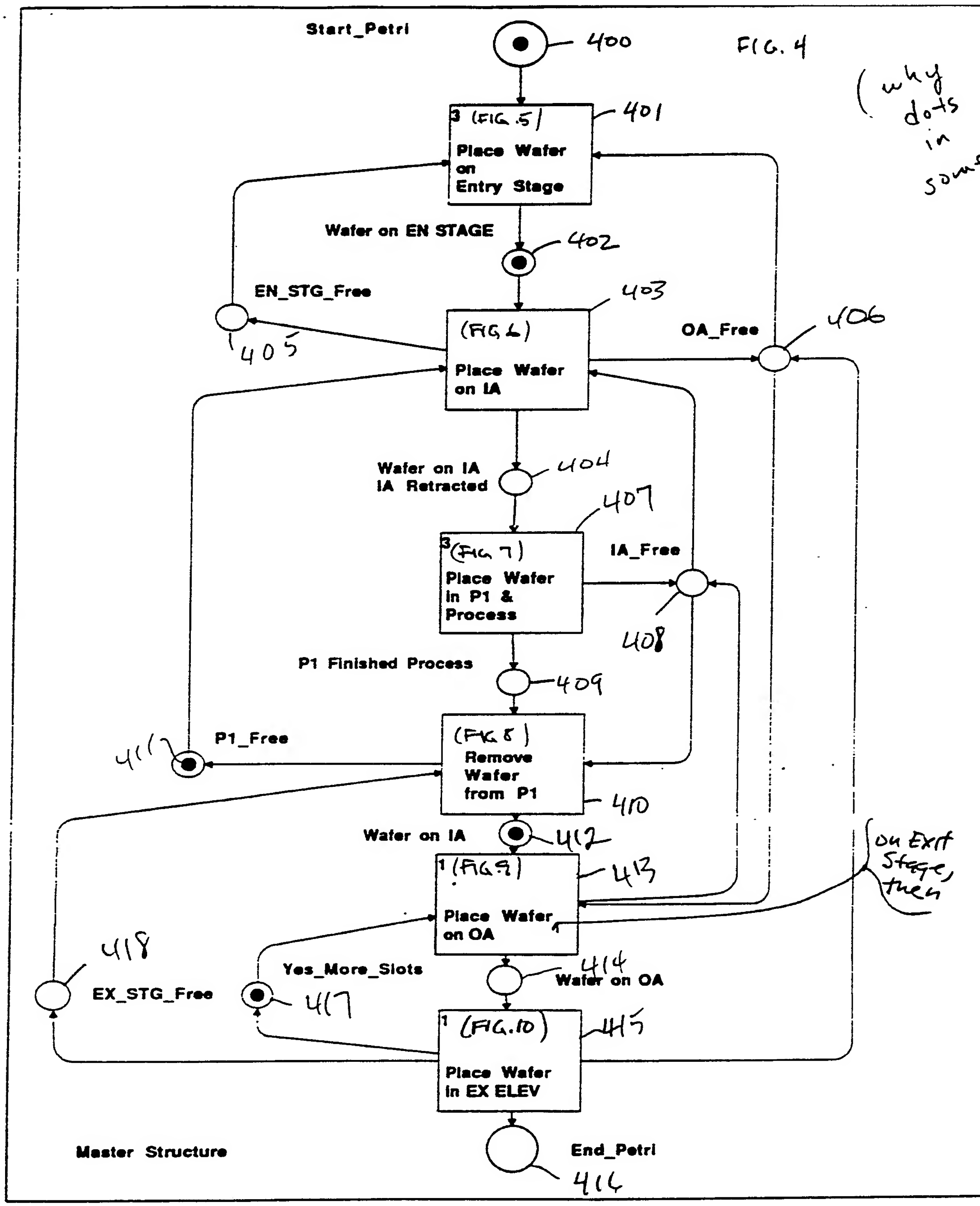


FIG 3


Start_Petri
400
FIG. 4
(why dots in some
3 (FIG. 5)
Place Wafer on Entry Stage
401
Wafer on EN STAGE
402
EN_STG_Free
405
403
(FIG 6)
Place Wafer on IA
OA_Free
406
Wafer on IA
IA Retracted
404
407
3 (FIG 7)
Place Wafer in P1 & Process
IA_Free
408
P1 Finished Process
409
(FIG 8)
Remove Wafer from P1
P1_Free
411
410
Wafer on IA
412
1 (FIG 9)
Place Wafer on OA
413
on Exit Stage, then
418
EX_STG_Free
Yes_More_Slots
417
414
Wafer on OA
1 (FIG.10)
Place Wafer in EX ELEV
415
Master Structure
End_Petri
416

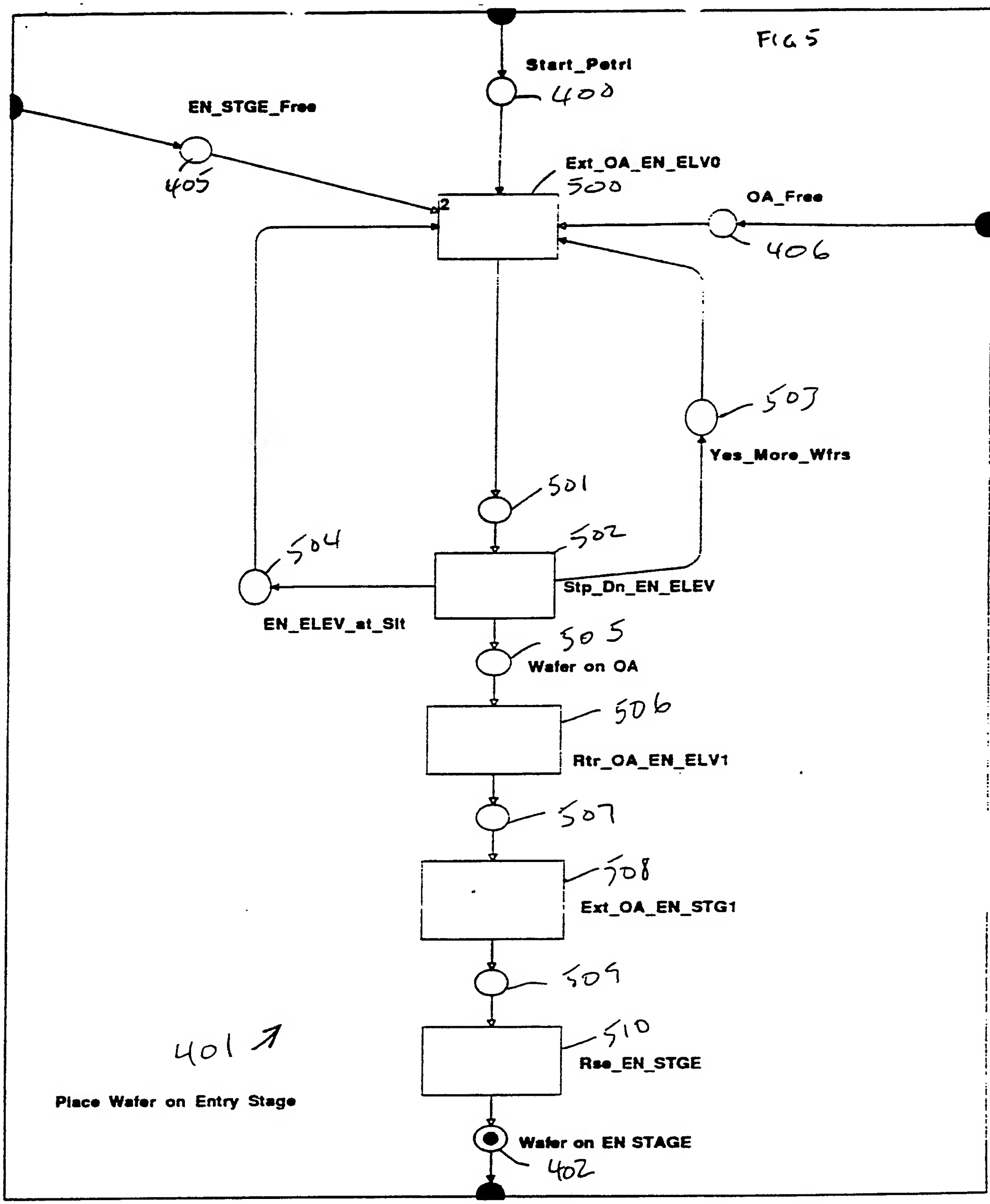


FIG 5
Start_Petri
400
EN_STGE_Free
405
Ext_OA_EN_ELV0
500
2
OA_Free
406
503
Yes_More_Wfrs
501
504
502
Stp_Dn_EN_ELEV
EN_ELEV_at_Slt
505
Wafer on OA
506
Rtr_OA_EN_ELV1
507
508
Ext_OA_EN_STG1
509
510
Rse_EN_STGE
401
Place Wafer on Entry Stage
Wafer on EN STAGE
402

FIG 6

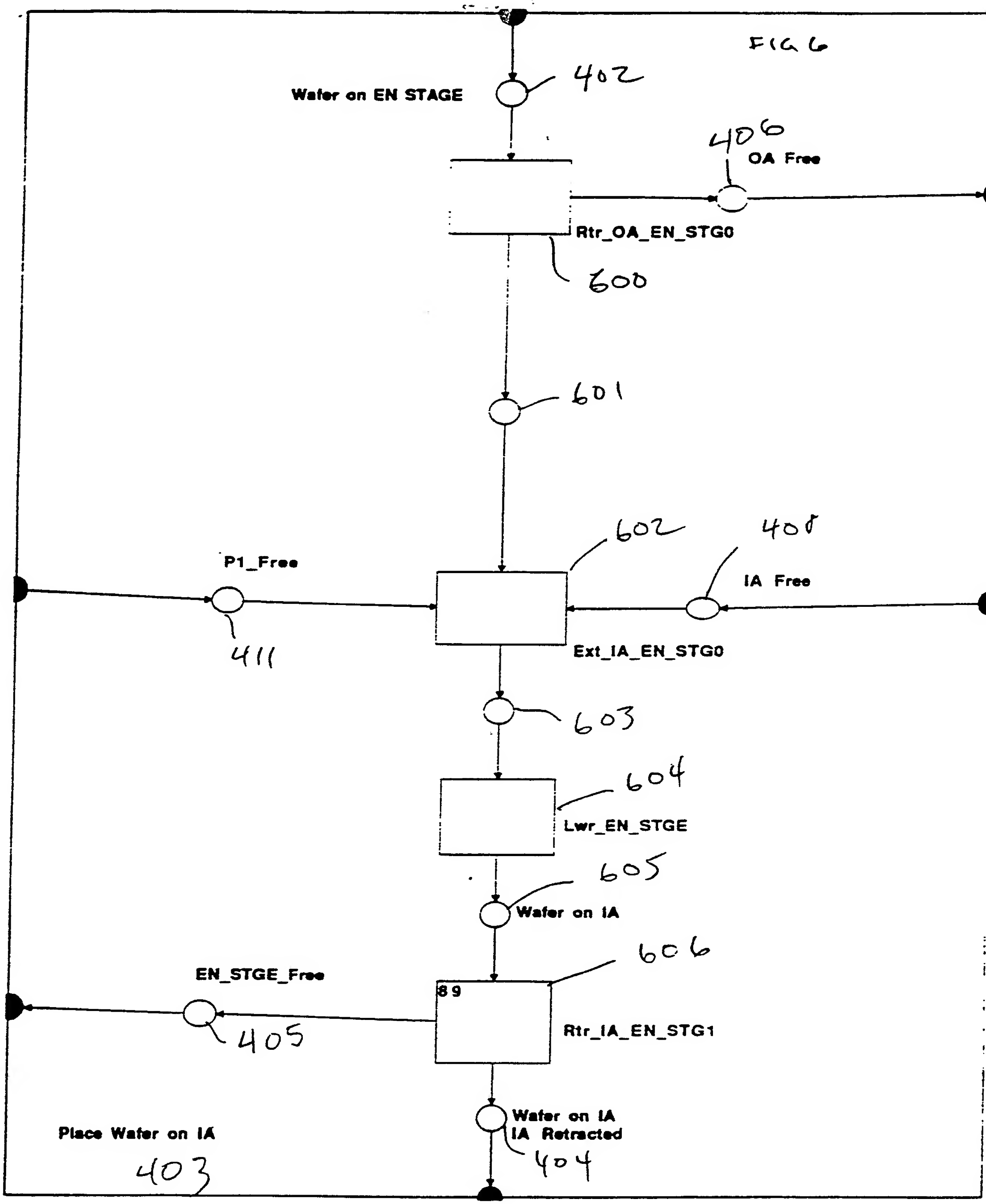

402
Wafer on EN STAGE
406
OA Free
Rtr_OA_EN_STG0
600
601
602
408
P1_Free
IA Free
411
Ext_IA_EN_STG0
603
604
Lwr_EN_STGE
605
Wafer on IA
606
EN_STGE_Free
89
Rtr_IA_EN_STG1
405
Wafer on IA
IA Retracted
Place Wafer on IA
403
404

FIG 7

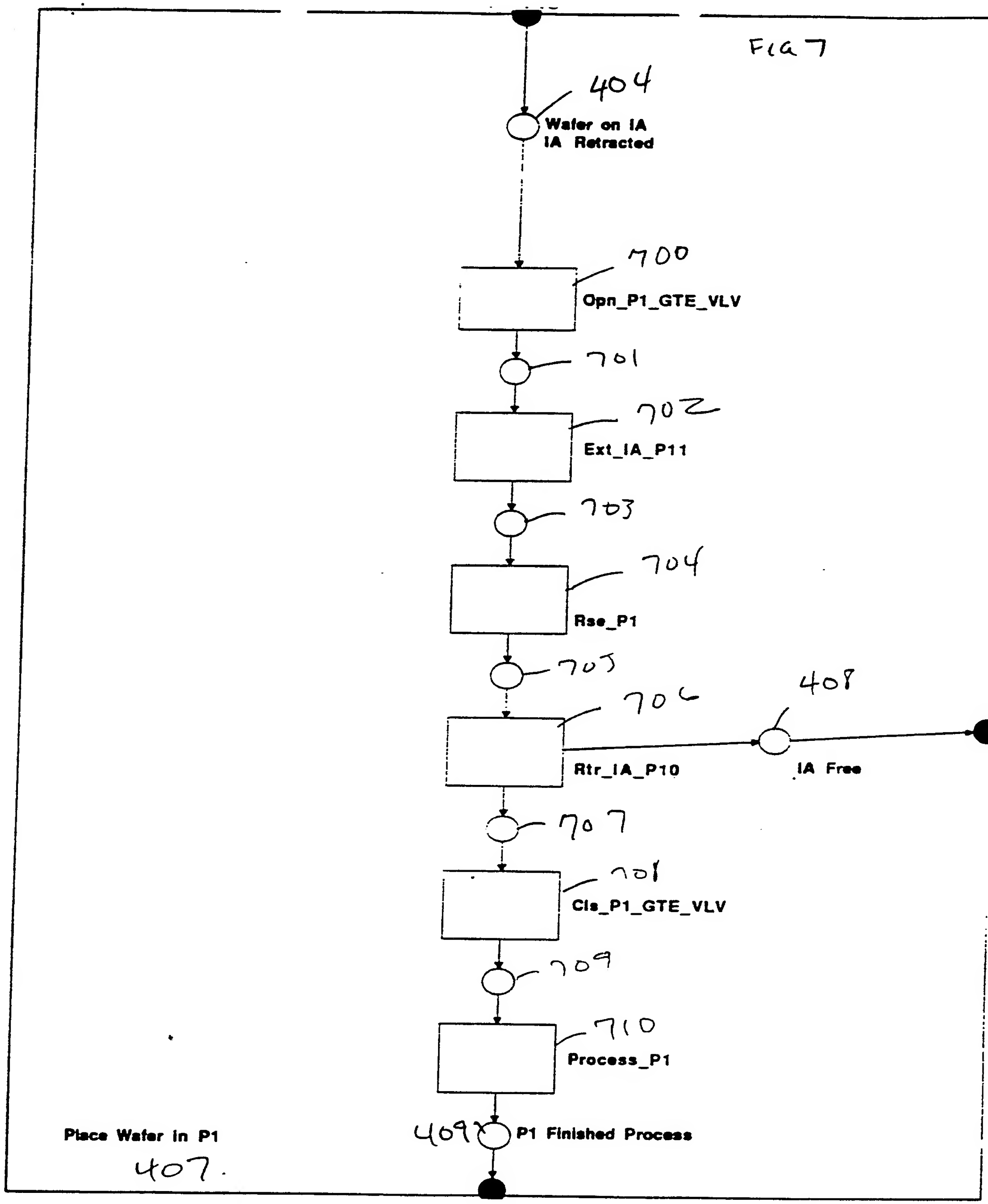
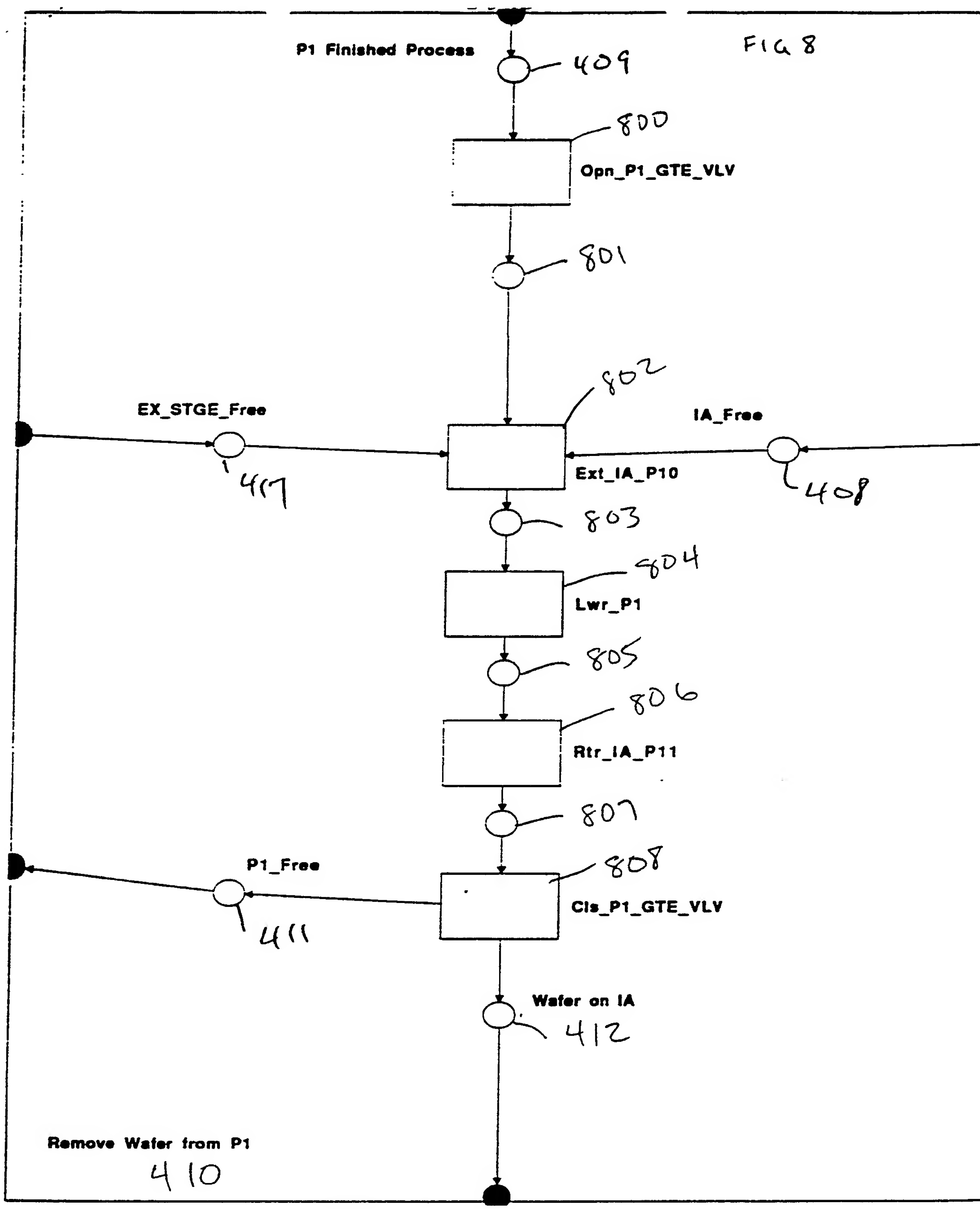

404
Wafer on IA
IA Retracted
700
Opn_P1_GTE_VLV
701
702
Ext_IA_P11
703
704
Rse_P1
705
706
408
Rtr_IA_P10
IA Free
707
708
Cls_P1_GTE_VLV
709
710
Process_P1
409
P1 Finished Process
Place Wafer in P1
407

FIG 8


P1 Finished Process
409
800
Opn_P1_GTE_VLV
801
802
EX_STGE_Free
IA_Free
Ext_IA_P10
417
408
803
804
Lwr_P1
805
806
Rtr_IA_P11
807
808
P1_Free
Cls_P1_GTE_VLV
411
Wafer on IA
412
Remove Wafer from P1
410

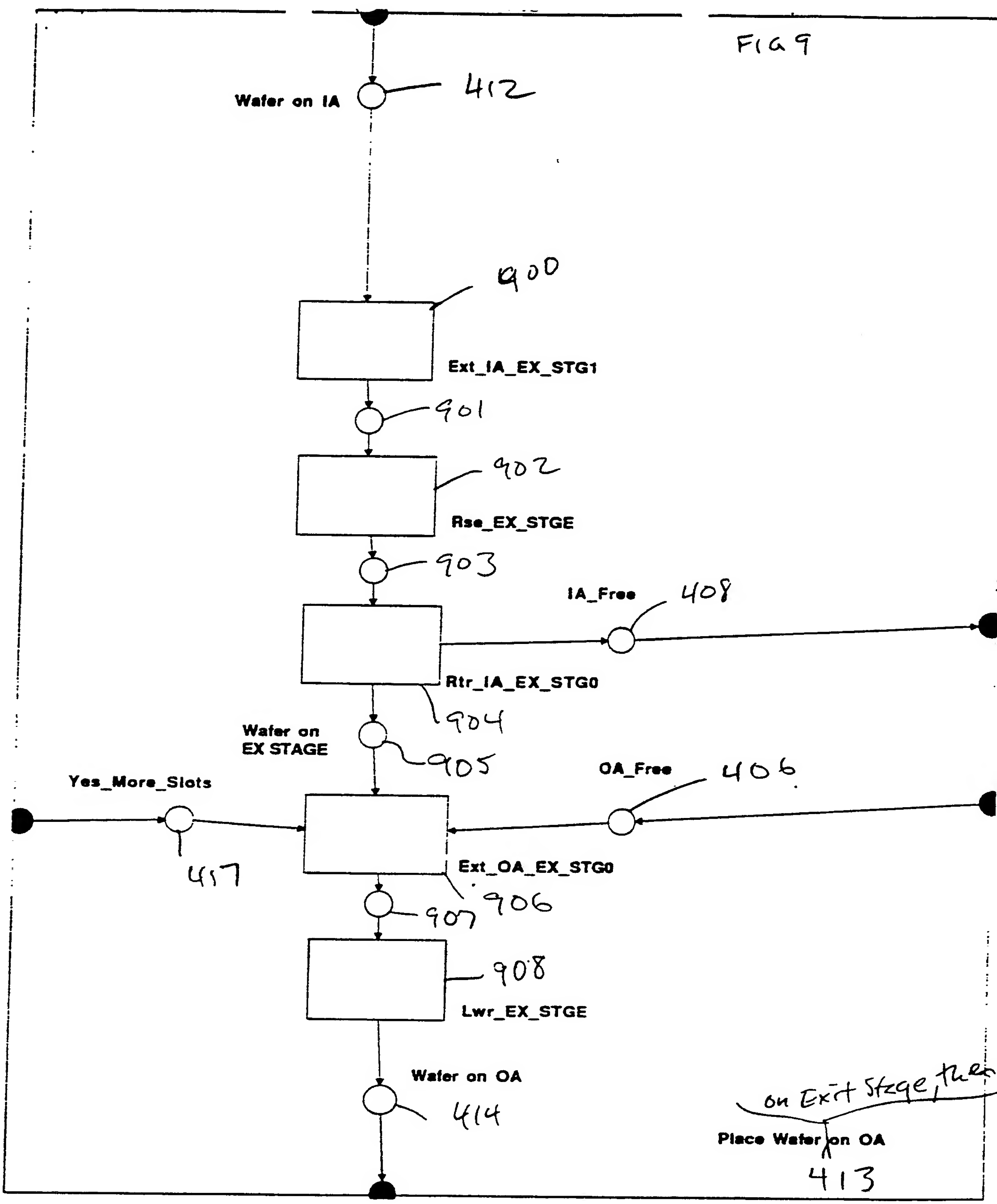


FIG 9
Wafer on IA
412
900
Ext_IA_EX_STG1
901
902
Rse_EX_STGE
903
IA_Free
408
Rtr_IA_EX_STG0
904
Wafer on
EX STAGE
905
Yes_More_Slots
OA_Free
406
417
Ext_OA_EX_STG0
906
907
908
Lwr_EX_STGE
Wafer on OA
414
on Exit Stage, then
Place Wafer on OA
413

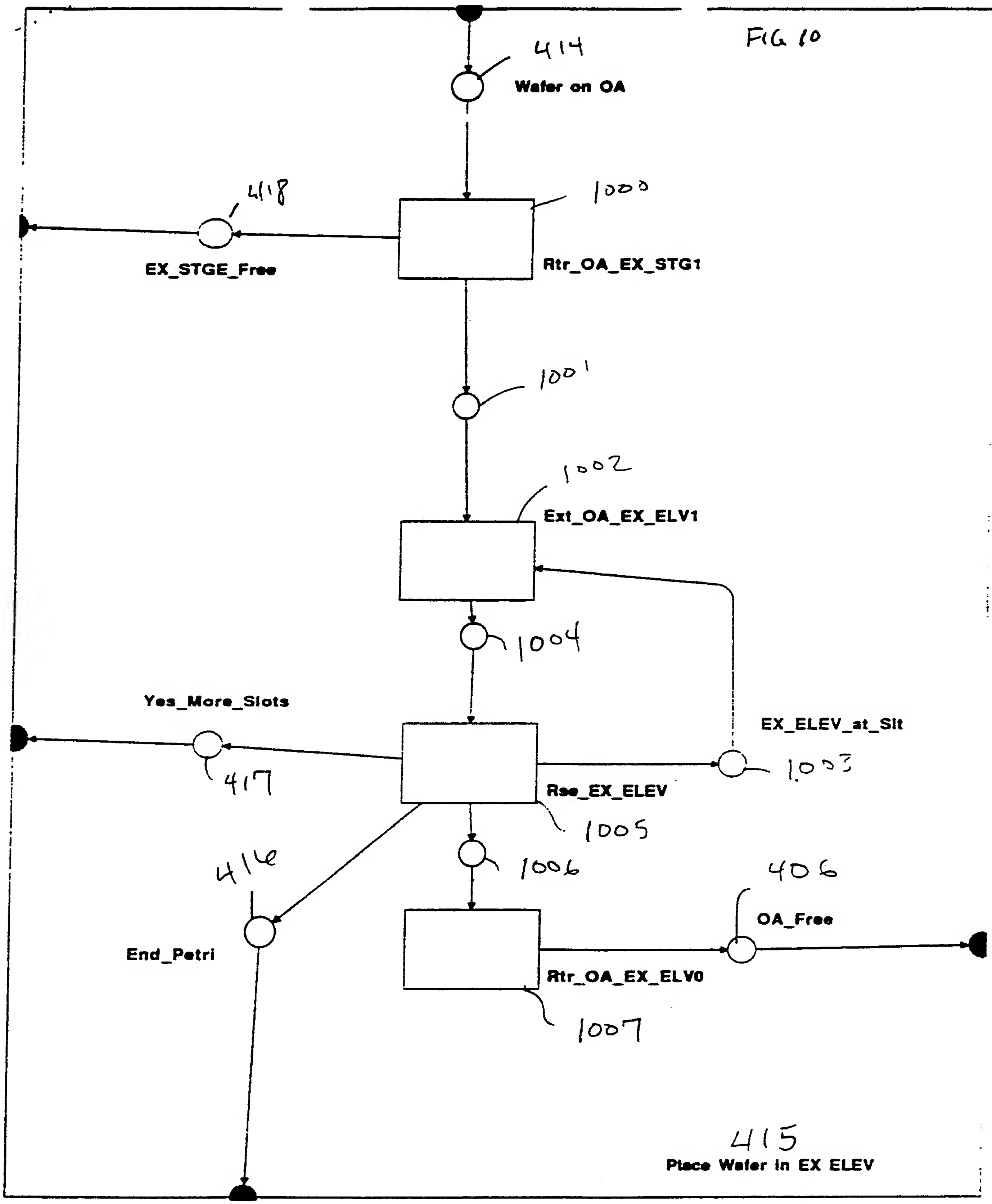


FIG 10
414
Wafer on OA
418
1000
EX_STGE_Free
Rtr_OA_EX_STG1
1001
1002
Ext_OA_EX_ELV1
1004
Yes_More_Slots
EX_ELEV_at_Slt
417
1003
Rse_EX_ELEV
1005
416
1006
406
OA_Free
End_Petri
Rtr_OA_EX_ELV0
1007
415
Place Wafer in EX ELEV

INTERNATIONAL SEARCH REPORT

International Application No PCT/US90/04877

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [3]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): B65G 49/07
U.S. CL.: 414/217

II. FIELDS SEARCHED

Minimum Documentation Searched [4]

Classification System	Classification Symbols
U.S.	414/217,221,222,225,935,939,940 901/8

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [5]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [14]

Category *	Citation of Document, [16] with indication, where appropriate, of the relevant passages [17]	Relevant to Claim No. [18]
Y	US, A, 4,825,808 (TAKAHASHI ET AL.) 02 May 1989, See Fig. 5.	1-19
Y	US, A, 4,715,764 (HUTCHINSON) 29 December 1987, See Fig. 3.	1-19
Y	US, A, 4,674,621 (TAKAHASHI) 23 June 1987, See Fig. 1.	1-19
Y	US, A, 4,722,298 (RUBIN ET AL.) 02 February 1988, See Col. 7, line 44-line 68.	2-4, 10-19
Y	US, A, 4,818,169 (SCHRAM ET AL.) 04 April 1989, See Col. 1, line 31-line 33.	3-4, 11-14
Y	US, A, 4,385,837 (SCHRAM) 31 May 1983, See Fig. 7.	13-14
Y	US, A, 4,687,542 (DAVIS ET AL.) 18 August 1987.	

* Special categories of cited documents: [15]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search [2]	Date of Mailing of this International Search Report [3]
18 OCTOBER 1990	04 FEB 1991
International Searching Authority [1]	**Signature of Authorized Officer [20]**
ISA/US	for Andre Robinson John VandenBosche

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

Y	US, A, 4,670,126 (MESSER ET AL.) 02 June 1987.	
A	US, A, 4,643,629 (TAKAHASHI ET AL.) 17 February 1987.	
A	US, A, 4,824,309 (KAKCHI ET AL.) 25 April 1989.	
A	US, A, 4,405,435 (TATEISHI ET AL.) 20 September 1983.	

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers ...., because they relate to subject matter [1] not required to be searched by this Authority, namely:

2. ☐ Claim numbers ...., because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [1], specifically:

3. ☐ Claim numbers ____________, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.
2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:
3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:
4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.